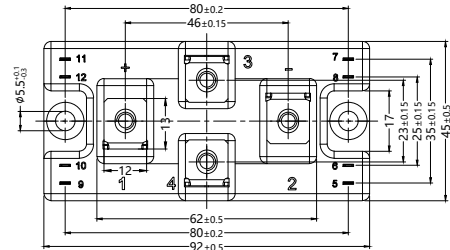
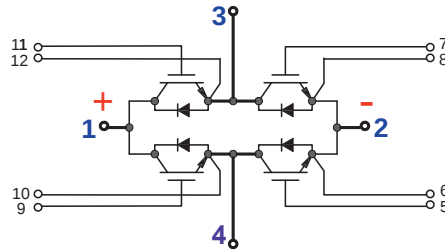
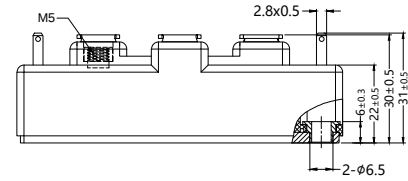


S4G50T120SC9

H bridge IGBT modules



Dimension: mm



$V_{CES} = 1200V$
 $I_{C100} = 4 \times 50A$
 $V_{CESat(typ)} = 1.90V$
 $E_{off(typ)} = 5.4mJ$

Absolute Maximum Ratings

Symbol	Test Conditions		Values	Unit
IGBT				
V _{CES}	T _j =25°C		1200	V
I _C	T _j = 175 °C	T _C =25°C	81	A
		T _C =100°C	50	A
I _{Cnom}	T _C = 100 °C Every chip		50	A
I _{CRM}	I _{CRM} = 3xI _{Cnom}		150	A
V _{GES}			-20 ... +20	V
tpsc	V _{CC} = 800 V V _{GE} ≤ 15 V V _{CES} ≤ 1200 V	T _j =150°C	10	μs
T _j			-40 ... 175	°C
Inverse diode				
I _F	T _j = 175 °C	T _C =25°C	50	A
		T _C =100°C	25	A
I _{Fnom}			25	A
I _{FRM}	I _{FRM} = 3xI _{Fnom}		75	A
I _{FSM}	t _p = 10 ms, sin 180°, T _j =25°C		90	A
T _j			-40 ... 150	°C
Module				
I _{t(RMS)}	T _{terminal} =80°C		200	A
T _{stg}			-40 ... 125	°C
V _{Isol}	AC sinus 50 Hz, t = 1 min		4000	V

Sirectifier®

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H bridge IGBT modules

Characteristics						
Symbol	Test Conditions		min.	typ.	max.	Unit
IGBT						
V _{CE(sat)}	I _C =50A	T _j =25°C		1.85	2.10	V
	V _{GE} =15V chiplevel	T _j =150°C		2.20	2.40	V
V _{CE0}	chiplevel	T _j =25°C		0.8	0.9	V
		T _j =150°C		0.7	0.8	V
r _{CE}	V _{GE} =15V	T _j =25°C		21.00	24.00	mΩ
	chiplevel	T _j =150°C		30.00	32.00	mΩ
V _{GE(th)}	V _{GE} =V _{CE} , I _C = 1.7 mA		5	5.8	6.5	V
I _{CES}	V _{GE} =0V	T _j =25°C			1	mA
	V _{CE} = 1200 V	T _j =150°C				mA
C _{ies}	V _{CE} =25V	f=1MHz		2.77		nF
C _{oes}	V _{GE} =0V	f=1MHz		0.20		nF
C _{res}		f=1MHz		0.16		nF
Q _G	V _{GE} = - 8 V...+ 15 V			280		nC
R _{Gint}	T _j =25°C			4.0		Ω
t _{d(on)}	V _{CC} = 600 V I _C =50A V _{GE} =±15V R _{G on} =8.2Ω R _{G off} =8.2Ω di/dt _{on} = 1700 A/μs di/ dt _{off} =670A/μs	T _j =150°C		98		ns
t _r		T _j =150°C		29		ns
E _{on}		T _j =150°C		5.5		mJ
t _{d(off)}		T _j =150°C		325		ns
t _f		T _j =150°C		75		ns
E _{off}		T _j =150°C		4.5		mJ
R _{th(j-c)}	per IGBT				0.53	K/W



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H bridge IGBT modules

Characteristics						
Symbol	Test Conditions		min.	typ.	max.	Unit
Inverse diode						
V _F = V _{EC}	I _F = 25A V _{GE} = 0 V chiplevel	T _j = 25 °C		2.22	2.54	V
		T _j = 150 °C		2.18	2.50	V
V _{F0}	chiplevel	T _j = 25 °C		1.3	1.5	V
		T _j = 150 °C		0.9	1.1	V
r _F	chiplevel	T _j = 25 °C		18.4	20.8	mΩ
		T _j = 150 °C		25.6	28.0	mΩ
I _{RRM}	I _F = 25A di/dt _{off} = 1380 A/μs V _{GE} = ±15 V V _{CC} = 600 V	T _j = 150 °C		25		A
Q _{rr}		T _j = 150 °C		8.7		μC
E _{rr}		T _j = 150 °C		3.8		mJ
R _{th(j-c)}	per diode				0.84	K/W
Module						
L _{CE}					30	nH
R _{CC'+EE'}	terminal-chip	T _C = 25 °C		0.65		mΩ
		T _C = 125 °C		1		mΩ
R _{th(c-s)}	per module			0.04	0.05	K/W
M _s	to heat sink M5		3		5	Nm
M _t		to terminals M5	2.5		5	Nm
						Nm
Weight					170	g

S4G50T120SC9

H bridge IGBT modules

Features

- Trench Field Stop technology
- Ultra fast free wheeling diodes technology
- Low switching losses
- Switching frequency up to 20KHz
- Positive temperature coefficient for easy parallelling
- MOS input, voltage controlled

Application

- Welding inverters

Advantages

- space and weight savings
- reduced protection circuits

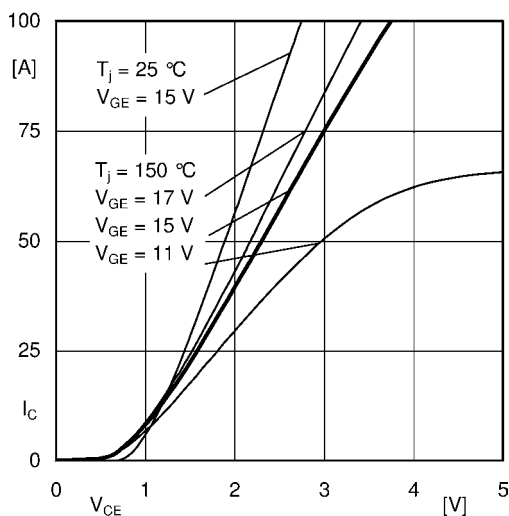


Fig. 1: Typ. output characteristic, inclusive $R_{CC} + EE'$

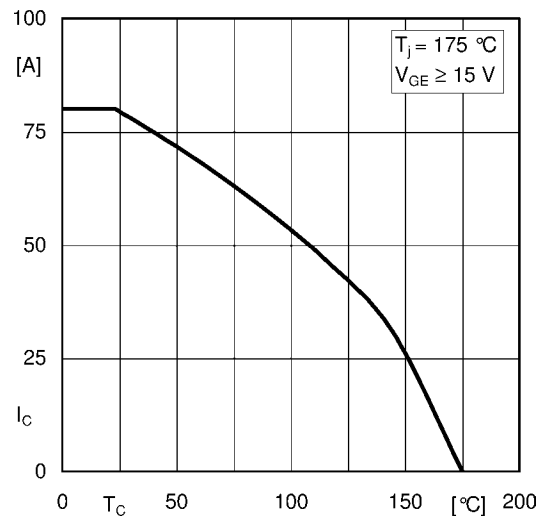


Fig. 2: Rated current vs. temperature $I_C = f(T_C)$

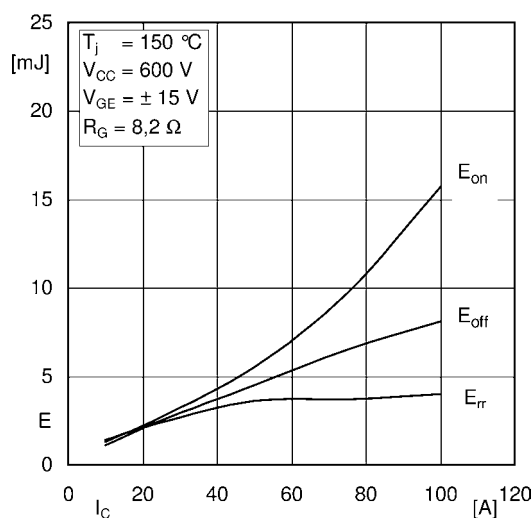


Fig. 3: Typ. turn-on /-off energy = $f(I_C)$

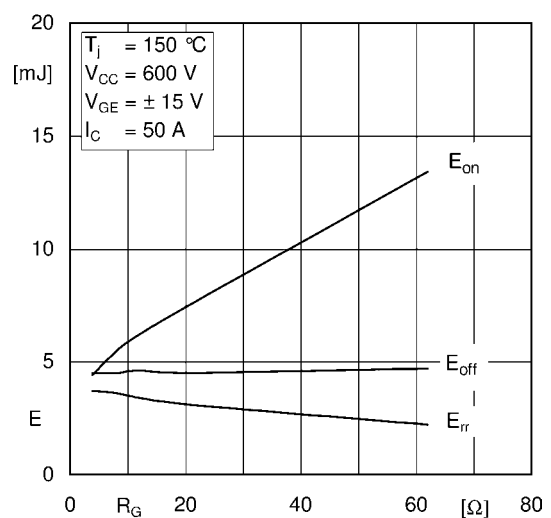


Fig. 4: Typ. turn-on /-off energy = $f(R_G)$

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H bridge IGBT modules

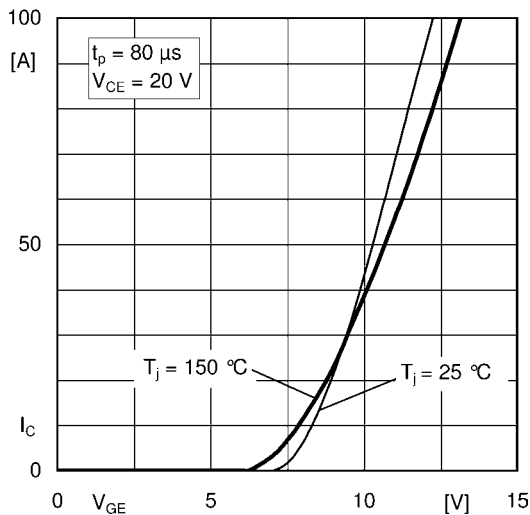


Fig. 5: Typ. transfer characteristic

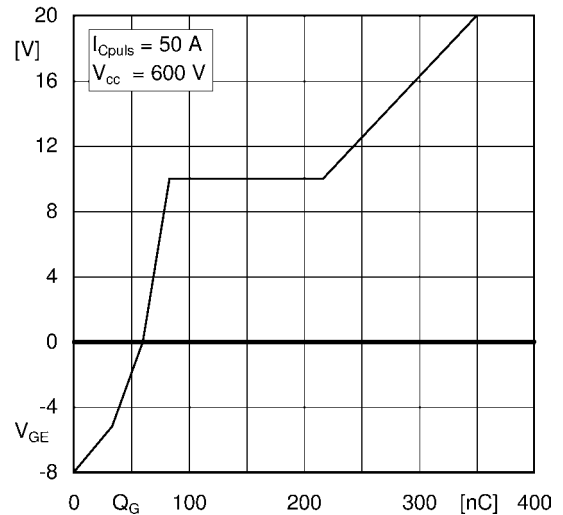


Fig. 6: Typ. gate charge characteristic

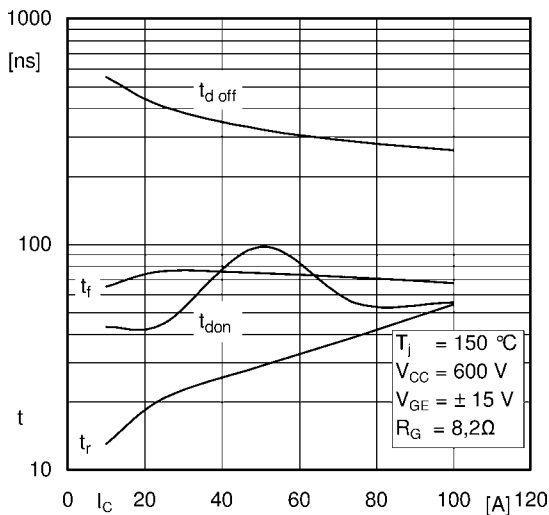


Fig. 7: Typ. switching times vs. I_C

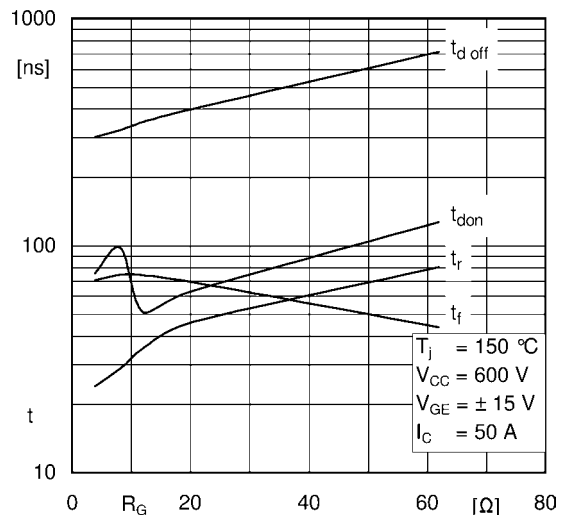


Fig. 8: Typ. switching times vs. gate resistor R_G

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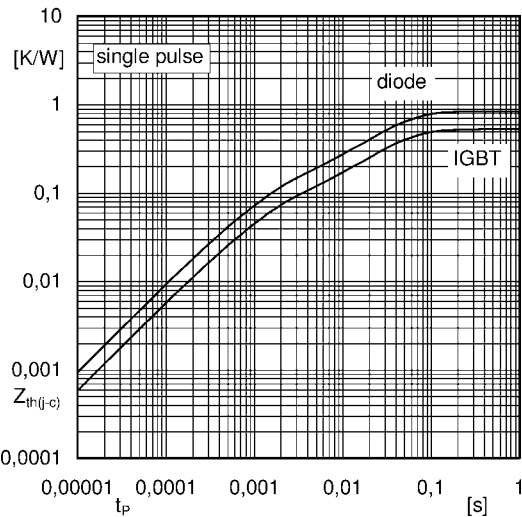


Fig. 9: Transient thermal impedance

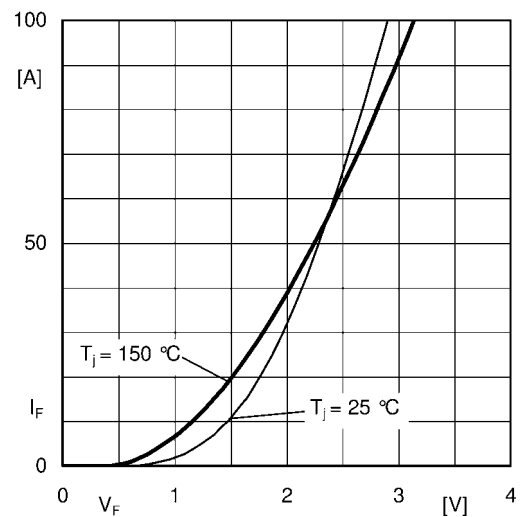


Fig. 10: Typ. FRD diode forward charact., incl. $R_{CC}+EE'$

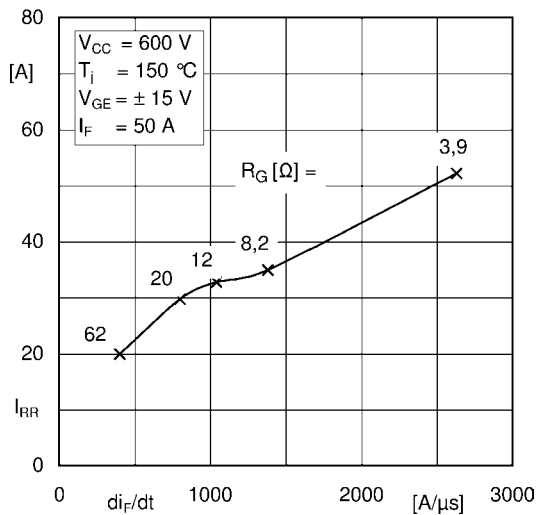


Fig. 11: FRD diode peak reverse recovery current

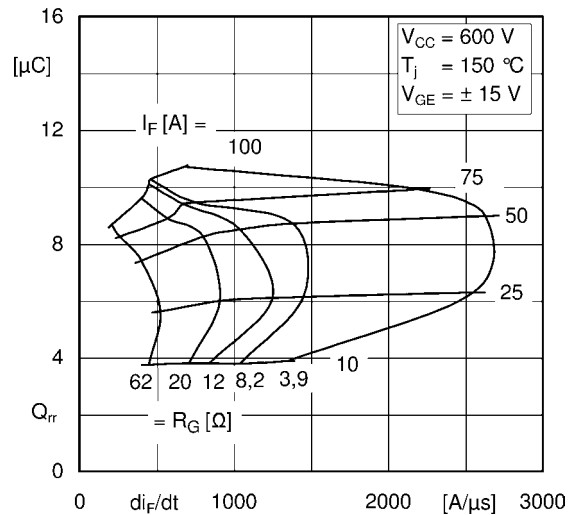


Fig. 12: Typ. FRD diode peak reverse recovery charge

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H bridge IGBT modules

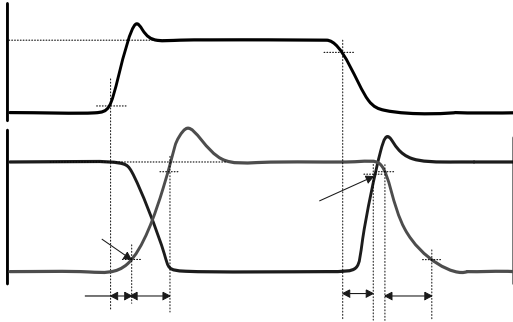


Figure A. Definition of switching times

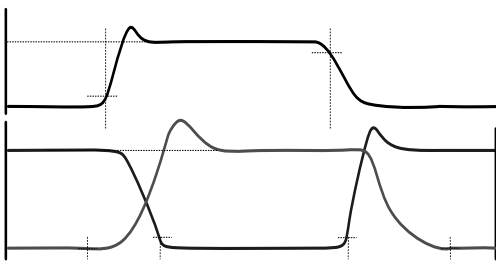


Figure B. Definition of switching losses

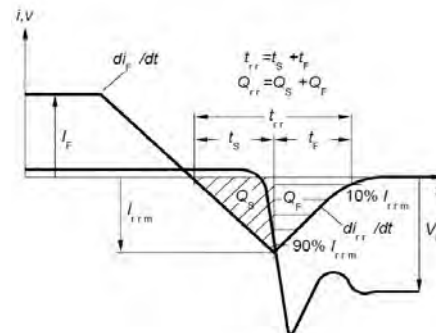


Figure C. Definition of diodes switching characteristics

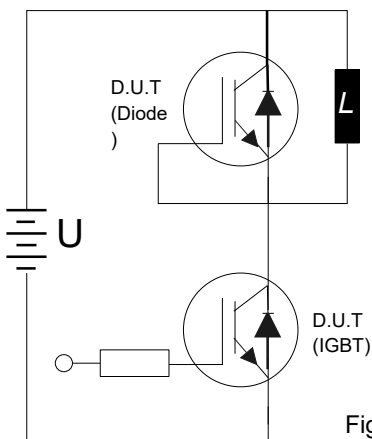


Figure D. Dynamic test circuit